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EXAMINER	
DARE, RYAN A	
ART UNIT	**PAPER NUMBER**
2186	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/631,988	Applicant(s) MARLAN ET AL.	
	Examiner Ryan Dare	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 20 November 2006.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-40 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-40 is/are rejected.

7)☒ Claim(s) 1-40 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see the appeal brief, filed 11/20/06 with respect to claims 1-40 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Hughes et al., US Patent 6427193 and Swami, US PGPub 2004/0165538.

Claim Objections

2. Claim 31 is objected to because of the following informalities: In the last line, "acknowledgments" is plural when it should be singular. Appropriate correction is required.

3. Claims 1-40 are objected to because they do not have a consistent spelling of the word "acknowledgment." While both "acknowledgment" and "acknowledgement" are proper spellings, Applicant should remain consistent with one spelling in the claims in order to avoid problems with lack of antecedent basis.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hughes et al., US Patent 6427193, in view of Swami, US PGPub 2004/0165538.

4. With respect to claim 1, Hughes et al. teach an apparatus comprising:

a load/store unit that includes a retry logic that is to retry access to a resource after receipt of a negative acknowledgement for an attempt to access the resource by the load/store unit, in col. 39, lines 20-32.

Hughes et al. fail to disclose the congestion detection logic of claim 1. Swami teaches a congestion detection logic to output a signal that indicates that the resource is congested based on receipt of a consecutive number of negative acknowledgements in response to access requests to the resource, in pars. 79 and 82

5. It would have been obvious to one of ordinary skill in the art, having the teachings of Hughes et al. and Swami. before him at the time the invention was made to combine the resource access apparatus of Hughes et al. with the resource access apparatus of Swami in order to eliminate deadlock problems and allow multiple processors to complete their memory operations as taught by Hughes et al. in the last three lines of the abstract.

6. With respect to claim 2, Swami teaches the apparatus of claim 1 further comprising a congestion control logic to disable the retry logic from retry accesses to the resource based on receipt of the signal from the congestion detection logic, in par. 14.

7. With respect to claim 3, Swami teaches to wait an amount of time while the resource is congested as discussed supra, but fails to teach an exponential delay. Hughes et al. teach an exponential delay in the abstract, where it says "the processor is configured to increase the backoff time at an exponential rate." The backoff time refers to the time before retrying to access the resource.

8. With respect to claim 4, Swami teaches the apparatus of claim 2, wherein the congestion control logic is to exponentially decrease the delay after the congestion detection logic receives a number of positive acknowledgements in response to access requests to the resource, in par. 66.

9. With respect to claim 5, Hughes et al. teach a processor comprising:

a functional unit to attempt to access data from memory coupled to the processor based on an access request, in figure 1 and col. 10, lines 1-2, wherein the functional unit is to retry attempts to access of the data based on other access of the data based on other access requests after receipt of a negative acknowledgement in response to the attempt to access the data, in col. 39, lines 20-32.

Hughes fails to teach the congestion detection logic of claim 5. Swami teaches a congestion detection logic to detect congestion of access of the data based on receipt

of a consecutive number of negative acknowledgments that exceed a threshold prior to access of the data, in pars. 79 and 82.

Hughes et al. teach a congestion control logic to disable the functional unit from attempts to access the data for a time period after the congestion is detected in col. 39, lines 6-23.

10. It would have been obvious to one of ordinary skill in the art, having the teachings of Hughes et al. and Swami. before him at the time the invention was made to combine the resource access apparatus of Hughes et al. with the resource access apparatus of Swami in order to eliminate deadlock problems and allow multiple processors to complete their memory operations as taught by Hughes et al. in the last three lines of the abstract.

11. With respect to claim 6, Hughes et al. teach the processor of claim 5, wherein the congestion control logic is to exponentially increase the time period after the congestion detection logic is to detect congestion while access to the other data in the memory is congested, in the abstract, where it says "the processor is configured to increase the backoff time at an exponential rate." The backoff time refers to the time before retrying to access the resource.

12. With respect to claim 7, Swami teaches the processor of claim 5, wherein the congestion control logic is to exponentially decrease the delay after the congestion detection logic receives a number of positive acknowledgements in response to access requests to the resource, in par. 66.

13. With respect to Claim 8, Hughes et al. teach a processor comprising:

a functional unit to attempt to access a cache line in a cache memory coupled to the processor based on an access request, in figure 1 and col. 10, lines 1-2, wherein the functional unit is to retry attempts to access of the data based on other access of the data based on other access requests after receipt of a negative acknowledgement in response to the attempt to access the data, in col. 39, lines 20-32.

a congestion control logic to disable the functional unit from attempts to access the data for a time period after the congestion is detected in col. 39, lines 6-23.

Hughes et al. fail to teach that the congestion detection logic is based on an average number of negative acknowledgements received that exceed a threshold prior to access of the data. Swami teaches using an average number of negative acknowledgements in par. 82

14. It would have been obvious to one of ordinary skill in the art, having the teachings of Hughes et al. and Swami. before him at the time the invention was made to combine the resource access apparatus of Hughes et al. with the resource access apparatus of Swami in order to eliminate deadlock problems and allow multiple processors to complete their memory operations as taught by Hughes et al. in the last three lines of the abstract.

15. With respect to claim 9, Swami teaches the processor of claim 8, wherein the average number of negative acknowledgements is within a window and wherein the congestion detection logic is to move the window over time of attempts, in pars. 79 and 82.

16. With respect to claim 10, Swami teaches the processor of claim 8, wherein the congestion control logic is to exponentially increase the time period after the congestion detection logic is to detect congestion while access of other cache lines in the cache memory is congested, in par. 66. Although the resource by Swami is not a cache line in a cache memory, Hughes et al. teach that the resource can be a cache line in a cache memory as discussed in the parent claim.

17. With respect to claim 11, Swami teaches the processor of claim 8, wherein the congestion control logic is to exponentially decrease the time period after the congestion detection logic receives a number of positive acknowledgements in response to attempts to access other cache lines in cache memory, in par. 66. Although the resource by Swami is not a cache line in a cache memory, Hughes et al. teach that the resource can be a cache line in a cache memory as discussed in the parent claim.

18. With respect to claim 12, Hughes et al. teach a system comprising:

a cache memory to store data, in fig. 25, L2 Cache 228; and

a first processor to attempt to access the data from the cache memory based on access requests, in fig. 25, Processor 10.

Hughes et al. fail to disclose the congestion detection logic of claim 12. Swami teaches a congestion detection logic to output a signal that indicates that the resource is congested based on receipt of a consecutive number of negative acknowledgements in response to access requests, in pars. 79 and 82.

19. It would have been obvious to one of ordinary skill in the art, having the teachings of Hughes et al. and Swami. before him at the time the invention was made to combine the resource access apparatus of Hughes et al. with the resource access apparatus of Swami in order to eliminate deadlock problems and allow multiple processors to complete their memory operations as taught by Hughes et al. in the last three lines of the abstract.

20. With respect to claim 13, Hughes et al. teach the system of claim 12 further comprising:

a second processor associated with the cache memory, in fig. 25, Processor 10a;

a hub controller to receive the access requests from the first processor, the hub controller to forward the access requests to the second processor, wherein the second processor is to determine whether the data in the cache memory is accessible, in fig. 25, Bus Bridge 202. The bus bridge acts as a hub controller in col. 43, lines 15-25.

21. With respect to claim 14, Hughes et al. teaches the system of claim 13, wherein the second processor is to transmit a negative acknowledgement back to the first processor through the hub controller if the data is not accessible, the second processor to transmit a positive acknowledgment back to the first processor through the hub controller if data is accessible, in col. 43, lines 15-25. Note that all requests are channeled through the bus bridge.

22. With respect to claim 15, Hughes et al. teach the system of claim 12, wherein the first processor further comprises a congestion control logic to disable the first processor

from transmitting the access requests if the congestion detection logic determines that access to the data is congested, in col. 39, lines 20-32.

23. With respect to claim 16, Hughes et al. teach the system of claim 12, wherein the congestion control logic is to disable the first processor from transmitting the access requests for a time period, wherein the time period is based on an exponential back off delay operation, in the abstract.

24. With respect to claim 17, Hughes et al. teach a system comprising:

a resource, in fig. 25, L2 Cache 228; and

a first processor having a load/store function unit, the load/store functional unit to attempt to access the resource based on access requests, in fig. 25, Processor 10 and fig. 2, Load/Store Unit 26.

Hughes et al. fail to disclose the congestion detection logic of claim 17. Swami teaches a congestion detection logic to detect congestion of access of the resource based on a consecutive number of negative acknowledgements received in response to the access requests prior to receipt of a positive acknowledgement in response to one of the access requests within a first time period, in pars. 79 and 82.

25. It would have been obvious to one of ordinary skill in the art, having the teachings of Hughes et al. and Swami before him at the time the invention was made to combine the resource access apparatus of Hughes et al. with the resource access apparatus of Swami in order to eliminate deadlock problems and allow multiple processors to complete their memory operations as taught by Hughes et al. in the last three lines of the abstract.

26. With respect to claim 18, Hughes et al. teach the system of claim 17, further comprising:

a second processor associated with the resource, in fig. 25, Processor 10a;

a hub controller to receive the access requests from the first processor, the hub controller to forward the access requests to the second processor, wherein the second processor is to determine whether the resource is accessible, in fig. 25, Bus Bridge 202. The bus bridge acts as a hub controller in col. 43, lines 15-25.

27. With respect to claim 19, Hughes et al. teaches the system of claim 18, wherein the second processor is to transmit a negative acknowledgement back to the first processor through the hub controller if the resource is not accessible, the second processor to transmit a positive acknowledgment back to the first processor through the hub controller if resource is accessible, in col. 43, lines 15-25, particularly the embodiment where the cache control logic is in the bus bridge, and controls the external cache.

28. With respect to claim 20, Hughes et al. teach the system of claim 17, wherein the first processor further comprises a congestion control logic to disable the load/store functional unit from attempting to access the resource if the congestion detection logic is to detect congestion of access of the resource, in col. 29, lines 20-32

29. With respect to claim 21, Hughes et al. teach the system of claim 17, wherein the congestion control logic is to disable the load/store unit from attempts to access the resource for a second time period, wherein the second time period is based on an exponential back off delay, in the abstract.

30. With respect to claim 22, Hughes et al. teach a system comprising:

a cache memory to include a number of cache lines for storage of data, in col. 39, lines 6-9.

At least two processors, wherein a first processor of the at least two processors is to attempt to access the data in one of the number of cache lines based on access requests, in col. 39, lines 6-9.

Hughes et al. fails to teach that the congestion detection logic to detect congestion of access of a first cache line of the number of cache lines based on a ratio of a number of negative acknowledgments to a number of positive acknowledgments received in response to the access requests. Swami teaches that the congestion logic can be any statistical parameter using negative and positive acknowledgments, in pars. 79-82.

31. It would have been obvious to one of ordinary skill in the art, having the teachings of Hughes et al. and Swami before him at the time the invention was made to combine the resource access apparatus of Hughes et al. with the resource access apparatus of Swami in order to eliminate deadlock problems and allow multiple processors to complete their memory operations as taught by Hughes et al. in the last three lines of the abstract.

32. With respect to claim 23, Hughes et al. teach the system of claim 22, wherein a second processor of the at least two processors is associated with the cache memory and wherein the system further comprises a hub controller, the hub controller to receive the access requests from the first processor, the hub controller to forward the access

requests to the second processor, wherein the second processor is to determine whether the one of the number of cache lines is accessible, in fig. 25, Processor 10a and Bus Bridge 202. The bus bridge acts as a hub controller in col. 43, lines 15-25.

33. With respect to claim 24, Hughes et al. teach the system of claim 23, wherein the second processor is to transmit a negative acknowledgement back to the first processor through the hub controller if the one of the number of cache lines is not accessible, the second processor to transmit a positive acknowledgement back to the first processor through the hub controller if the one of the number of cache lines is accessible, in col. 43, lines 15-25. Note that all requests are channeled through the bus bridge.

34. With respect to claim 25, Hughes et al. teach the system of claim 22, wherein the first processor further comprises a congestion control logic to disable, for a time period, the first processor to attempt to access the data if the congestion detection logic is to detect congestion of access of the first cache line, in col. 39, lines 20-32.

35. With respect to claim 26, Hughes et al. teach the system of claim 25, wherein the congestion control logic is to exponentially increase the time period after the congestion detection logic is to detect congestion while access to other cache lines in the cache memory, in the abstract.

36. With respect to claim 27, Hughes et al. teach a method comprising:

transmitting access requests, by a first processor, to access data in a memory, in col. 39, lines 6-9;

Hughes fails to teach the congestion detection logic based on a consecutive number of negative acknowledgments. Swami teaches receiving, by the first processor,

a positive acknowledgement or a negative acknowledgment from a second processor that is associated with the memory based on the number of access requests, in pars. 79 and 82; and

detecting congestion of the data based on receipt, by the first processor, of a consecutive number of negative acknowledgements that exceed a first threshold, prior to receipt, by the first processor, of a positive acknowledgment, in pars. 79 and 82.

37. It would have been obvious to one of ordinary skill in the art, having the teachings of Hughes et al. and Swami before him at the time the invention was made to combine the resource access apparatus of Hughes et al. with the resource access apparatus of Swami in order to eliminate deadlock problems and allow multiple processors to complete their memory operations as taught by Hughes et al. in the last three lines of the abstract.

38. With respect to claim 28, Hughes et al. teaches controlling access to the data in the memory in col. 39, lines 20-32, but fails to teach that it is due to a consecutive number of negative acknowledgements, received by the first processor, exceeds the first threshold, prior to receipt of the positive acknowledgement. Swami teaches receiving a consecutive number of negative acknowledgements, prior to receiving a positive acknowledgement in pars. 79 and 82.

39. With respect to claim 29, Hughes et al. teaches the method of claim 28, wherein controlling access to the data in the memory comprises disabling transmitting of the access requests, by the first processor, for a time period, in col. 39, lines 20-32.

40. With respect to claim 30, Hughes et al. teaches the method of claim 29, wherein controlling access to the resource comprises exponentially increasing the time period upon determining that the congestion is detected for other data in the memory while the time period has not expired, in col. 39, lines 20-32

41. With respect to claim 31, Hughes et al. teaches a method comprising:

accessing, by at least one processor, a resource based on an access request, in col. 39, lines 26-69;

Hughes fails to teach the congestion detection logic based on the consecutive number of negative acknowledgements.. Swami teaches:

receiving a positive acknowledgement if the resource is accessible, in pars. 64-65;

receiving a negative acknowledgement if the resource is not accessible, in pars. 79 and 82;

retrying accessing, by the at least one processor, of the resource based on a number of access requests, in pars. 64-65.

detecting that a consecutive number of negative acknowledgements exceeds a first threshold within a time period, prior to receiving a positive acknowledgment, in pars. 79 and 82.

42. It would have been obvious to one of ordinary skill in the art, having the teachings of Hughes et al. and Swami before him at the time the invention was made to combine the resource access apparatus of Hughes et al. with the resource access apparatus of Swami in order to eliminate deadlock problems and allow multiple

processors to complete their memory operations as taught by Hughes et al. in the last three lines of the abstract.

43. With respect to claim 32, Hughes et al. teaches controlling access to the resource by the at least one processor, in col. 39, lines 20-32, but fails to teach that the controlling of access has to do with the receipt of a consecutive number of negative acknowledgments. Swami. teaches the congestion detection logic based upon the consecutive number of negative acknowledgements, exceeds the first threshold, prior to receipt of the positive acknowledgement, in pars. 79 and 82.

44. With respect to claim 33, Hughes et al. teach the method of claim 31, wherein controlling access to the resource comprises disabling transmitting of the access requests, by the first processor, for a time period, in col. 29, lines 20-32.

45. With respect to claim 34, Hughes et al. teach a computer storage medium that provides instructions, which when executed by a machine, cause said machine to perform operations comprising:

transmitting access requests, by a first processor, to access data in a memory, in col. 39, lines 6-9;

Hughes fails to teach the congestion detection logic based on consecutive number of negative acknowledgments. Swami teaches:

receiving, by the first processor, a positive acknowledgement or a negative acknowledgment from a second processor that is associated with the memory based on one of the number of access requests, in pars. 79-82.

detecting congestion of the data based on receipt, by the first processor, of a consecutive number of negative acknowledgements that exceed a first threshold, prior to receipt, by the first processor, of a positive acknowledgment, in pars. 79-82.

46. It would have been obvious to one of ordinary skill in the art, having the teachings of Hughes et al. and Swami before him at the time the invention was made to combine the resource access apparatus of Hughes et al. with the resource access apparatus of Swami in order to eliminate deadlock problems and allow multiple processors to complete their memory operations as taught by Hughes et al. in the last three lines of the abstract.

47. With respect to claim 35, Hughes et al. teaches controlling access to the data in the memory in col. 39, lines 20-32, but fails to teach that it is due to a consecutive number of negative acknowledgements, received by the first processor, exceeds the first threshold, prior to receipt of the positive acknowledgement. Swami teaches receiving a consecutive number of negative acknowledgements, prior to receiving a positive acknowledgement in pars. 79 and 82.

48. With respect to claim 36, Hughes et al. teaches the computer storage medium of claim 35, wherein controlling access to the data in the memory comprises disabling transmitting of the access requests, by the first processor, for a time period, in col. 39, lines 20-32.

49. With respect to claim 37, Hughes et al. teaches the computer storage medium of claim 36, wherein controlling access to the resource comprises exponentially increasing

the time period upon determining that the congestion is detected for other data in the memory while the time period has not expired, in col. 39, lines 20-32

50. With respect to claims 38-40, Applicant claims a computer storage medium that provides instructions which performs the method of claims 34-36 and is therefore rejected using similar logic.

Conclusion

51. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan Dare
March 18, 2007

PIERRE BATAILLE
PRIMARY EXAMINER
03/19/07